

Systems Architecture of the English Electric KDF9 computer.

This transistor-based machine was developed by an English Electric team under ACD Haley, of which the leading light was RH Allmark – (see section N4X5 for a full list of technical references). The KDF9 was remarkable because it is believed to be the first zero-address instruction format computer to have been announced (in 1960). It was first delivered at about the same time (early 1963) as the other famous zero-address computer, the Burroughs B5000 in America. A zero-address machine allows the use of *Reverse Polish* arithmetic; this offers certain advantages to compiler writers.

It is believed that the attention of the English Electric team was first drawn to the zero-address concept through contact with *George* (General Order Generator), an autocode programming system written for a Deuce computer by the University of Sydney, Australia, in the latter half of the 1950s. *George* used Reversed Polish, and the KDF9 team was attracted to this convention for the pragmatic reason of wishing to enhance performance by minimising accesses to main store. This may be contrasted with the more theoretical line taken independently by Burroughs.

To quote Bob Beard's article in the autumn 1997 issue of *Resurrection*, the KDF9 had the following architectural features:

- Zero Address instruction format (a first?);
- Reverse Polish notation (for arithmetic operations);
- Stacks used for arithmetic operations and Flow Control (Jumps) and I/O using ferrite cores with a one microsecond cycle;
- Separate Arithmetic and Main Controls with instruction prefetch;
- Hardware Multiply and Divide occupying a complete cabinet with clock doubled;
- Separate I/O control;
- A word length of 48 bits, comprising six 8-bit 'syllables' (the precursor of the byte). These syllables comprised a 2-bit field plus two 3-bit fields, coded in what was termed 'slob-octal' (syllabic octal).
- A 6-bit character set (plus 2 bits for parity, for I/O only!) which gave eight characters per KDF9 word;
- Variable Length instructions comprising one, two or three syllables (thus the KDF9 word could contain six arithmetic instructions, two main store operations, three two syllable instructions or any mix): instructions could span word boundaries but a special compiler feature could force a new word if required.
- The 48-bit word could contain the following arithmetic formats:
 - one 48-bit fixed point (signed) number;
 - two half-length fixed point numbers;
 - half of one double-length fixed point number;
 - one 48-bit floating point number (39-bit fraction, 8-bit characteristic, 1-bit sign);
 - two half-length floating point numbers;

- half of one double-length floating-point number;
- The 48-bit word could contain eight 6-bit characters.
- Microcoded instruction sequences based on two interlaced clocks (P1 and P2) running at 1 MHz, a pulse width of 250 nanoseconds, the machine being 'synchronous', and a minimum instruction time of one microsecond.
- A main store with a six microsecond cycle time (48 bits) up to eight times 4096 words with no parity! (equivalent to 196K bytes).
- An internal register structure, consisting of a 16 word by 48 bit arithmetic 'stack', the 'Nesting Store', a separate 16-word nesting store for subroutine return addresses, a 16-word (the 48 bits organised as 3x16 bits) 'Q' store used for I/O and address modification operations [all quadrupled for the optional Time Sharing feature], all with a cycle time of one microsecond but NO parity!
- A physical technology using single sided printed circuit boards of approximately 6 inches by 8 inches, with 24 pcbs per 'bin', eight bins per 'rack', and two racks per 'cubicle'.
- Use of high speed transistors, transformer coupled, diode-transistor logic [+ nor gates], several MAD (multi aperture devices) for complex logic conditions, diode matrix sequencers;
- A typical pcb, the BIFF (flip-flop), four per board, using eight transistors and discretes, with 32 gold plated edge fingers;
- As a rough approximation, 20,000 transistors per KDF9 system, and 2000 transformers (Polo sized toroids);
- A single phase Swinging Choke stabilised Power Supply generating ~750 amps at 5 volts +/-12v, +/-5v...

To quote Bill Findlay at: <http://www.findlayw.plus.com/index.html#HeadingKDF9> : The KDF9 was one of the earliest fully hardware-secured multiprogramming systems. Up to four programs could be run at once under the control of its elegantly simple operating system, the EE Timesharing Director. Each was confined to its own core area by hardware relocation. A program had its own sets of working registers, which were activated when that program was dispatched, so that context switching was efficient. A program could drive hardware I/O devices directly, but was limited by hardware checks to those that the Director had allocated to it. Any attempt to use an unallocated device, or to access unallocated core store, caused an error interrupt. There was hardware-enforced mutual exclusion of access to I/O buffers. When a program blocked for that reason, or by voluntarily waiting for an I/O transfer to terminate, it was interrupted and Director switched to the program of highest priority that was not itself blocked. When a blockage cleared, and the newly unblocked program was of higher priority than the program currently running, an interrupt to Director allowed for an immediate context switch.

Later operating systems included multi-access features, usually with PDP-8 front ends to handle the interactive terminals. They included Eldon 2, at the University of Leeds; and Egdon, COSEC and COTAN, developed primarily at UKAEA Culham Laboratories. The EE Kidsgrove and Whetstone Algol 60 compilers were among the first of their class.

English Electric produced a 34-page illustrated brochure in about 1961 that gives a good technical overview of the KDF9 system. This document is available on-line at:
http://www.ourcomputerheritage.org/KDF9_Flier.pdf