Version 2 January 2022. **N3X3**

Instruction sets of the English Electric KDP10 and KDF8 computers.

KDP10.

Information taken from *KDP10 Programming Manual. English Electric publication 1022. Undated but probably 1961. 198 pages.* Information on the KDF8 follows on below.

Instructions.

The KDP10's repertoire consists of 49 separate instructions. Each instruction is eight characters (16 octal digits) long and is in the two-address format. Instructions are stored in HSM in two successive tetrads. Instruction-fetch therefore takes 30 microsecs (two memory cycles).

The instruction layout is: <op code> <A-address> <N code> <B address> , where:

<op code> = two octal digits

<A-address> = six octal digits; usually a High Speed Memory (HSM) address of an operand (tetrad) or the left boundary of an operand.

<N code> = two octal digits; permitting automatic modification of an A- and/or B- address via any of the seven (four static and three dynamic) Address Modifiers.

<B-address> = six octal digits; usually a HSM address of an operand (tetrad) or the right boundary.

For some instructions, each of the three characters of the A or B address may separately signify something. In these cases, the constituent components are referred to as A1, A2, A3 and B1, B2, B3.

Address modification.

A dedicated area of HSM is used in place of separate modifier registers.

Octal digit in the N field	***Location of modifier***
0	No modifier
1	HSM locations 000111 -> 000113
2	HSM locations 000221 -> 000223 (STA)
3	HSM locations 000131 -> 000133
4	Use the P register
5	HSM locations 000151 -> 000153
6	Use the T register
7	HSM locations 000171 -> 000173

Summary of standard HSM locations used for dedicated purposes.

HSM locations	*Use*
000001 – 000003	The Return After Interrupt (RAI) instruction uses these.
000004 – 000017	Used as temporary space by arithmetic instructions
000020 – 000037	Used by read and write instructions
000040 – 000047	Rollback entrance, normal.
000050 – 000057	Rollback entrance, simultaneous mode.
000111 – 000173	Used for address modification (see separate table)
000200	Control transferred to this address if a Paper Advance is sensed (SSM instruction) in the Simultaneous Mode
000221 – 000223	STA and AM2
000241 – 000243	STP

Summary of the KDP10 instruction repertoire.

Input/output instructions.
These work with the following on-line peripherals: magnetic tape, paper tape reader and punch, monitor printer, on-line printer. Read instructions are stored in standard HSM locations 000020 -> 000027, thus being available for the Rollback routine if an error occurs.

Data-handling instructions.
These manipulate data stored in HSM.

Arithmetic instructions.
There are four instructions for decimal arithmetic, five for binary arithmetic and two instructions for altering the bit configuration of an operand via the logical operations AND, OR. The decimal instructions are designed to handle operands of unequal and practically unlimited length by aligning the least-significant digits of the operands. The instructions are able to recognize control symbols such as ISS (item separator symbol). Therefore the need for programmers to pre-position operands is eliminated. The binary instructions handle operands of equal but unlimited length, length being defined by address specification. Pre-alignment is necessary.

Decision and control instructions.
In this category are seven instructions which influence the direction of execution of a program. Four of these are conditional control transfers, using the PRIs (the three previous result indicators) or the state of the simultaneous mode or the status of a designated magnetic tape station. Two instructions are unconditional. The final instruction enables the computer to execute the same subroutine any designated number of times. There are five more special instructions. Two of these enable programmers to address registers directly, one controls the Simultaneous Gate and two instructions halt the computer (one with and one without error indication).

The complete list of the 49 KDP10 instructions follows. Note that some op code combinations are unassigned; these are left blank in the Table below.

Op code	*Mnemonic*	*Instruction*	*Comments*
00			
01	PES	Program error stop	
02	PR	Print	Print one 120-char line
03	PA	Paper advance	Newline on the lineprinter
04	LRR	Linear read reverse	Transfers a message from mag tape or paper tape to HSM.
05	BRR	Block read reverse	Ditto, transferring a block of characters
06	UNS	Unwind n symbols	Moves a selected mag tape forward until a specified number of a designated symbol has been counted
07			
10	TCW	Transcribing card punch write	Same as LW but at half speed (16.7 KC)
11	SSW	Single sector write	Write a sector of any size in block format from HSM to either mag tape or the Monitor Printer.
12	LW	Linear write	Transfers a message from HSM to mag tape, the Monitor Printer or paper tape.
13	MSW	Multiple sector write	Transfers to mag tape (or Monitor Printer) a Block comprising the contents of any Number of sectors taken from the HSM Under the direction of a stored list of Addresses.
14	LRF	Linear read forward	Reads one message from mag tape or Paper tape to HSM.
15	BRF	Block read forward	Reads a block of characters from mag tape Or paper tape to HSM.
16	RNS	Rewind n symbols	Causes a selected mag tape to be moved Backward by a specified number of Symbols.
17	RWD	Rewind to BTC	Causes a selected mag tape to be Completely rewound.
20			
21	IT	Item transfer	Transfers an item from one group of Successive HSM locations to another.
22	OCT	One character transfer	Transfers the contents of one HSM Location into another HSM location.
23			
24	STC	Sector transfer by character	Transfers a series of characters from an Area (sector) between, and including, two Designated HSM locations to another HSM Area (sector).
25	TCT	Three character transfer	Transfers, in parallel, the contents of the Right-most three locations of one tetrad to The right-most three locations of another

			Tetrad in HSM.
26	STT	Sector transfer by tetrad	Transfers the contents of one tetrad or any Number of consecutive HSM tetrads between, and including, two specified tetrad Addresses into another specified tetrad or Consecutive series of tetrads.
27	RD	Random distribute	Distributes successive items in the HSM, to locations specified by a stored list of addresses.
30			
31	LNS	Locate nth symbol in sector	Searches the contents of successive HSM locations between, and including, two give addresses, counting the occurrences of a designated symbol.
32	ZS	Zero suppress	Deleted the non-significant zeros to the left of the MSC of the result of a decimal arithmetic operation.
33	JR	Justify right	Gives right columnar alignment by: (a) adjusting and transferring an item from one series of successive HSM locations to another, or (b) adjusts the item, leaving it in the same group of HSM locations.
34	SCC	Sector clear by character	Places space characters in all the locations between, and including, two HSM addresses.
35	SCR	Sector compress – retain redundant ISS's	Transfers a sector of characters from one part of the HSM to another, in the process removing all spaces located to the right of the right-most non-space character within each item in the sector.
36	SCT	Sector clear by tetrad	Inserts spaces in the HSM locations between, and including, two given tetrad addresses. (Clears four characters at a time).
37	SCD	Sector compress – delete redundant ISS's	Transfers a sector of data from one part of HSM to another. In the process it deletes: (a) all ISSs originally located to the right of the right-most non-ISS, non-space character in the sector, and (b) all spaces located to the right of the right-most non-space character in the sector.
40			
41	BA	Binary add	The operands (assumed numeric) may be of any length but must have the same length.
42	BS	Binary subtract	Ditto
43	SC	Sector compare	Determines the relative magnitude of two operands of equal length. Sets the PRI bits accordingly.
44	TCA	Three character add	Binary addition of an augend stored in the right-most three locations of a tetrad and a three-character augend. The result is automatically stored in the locations previously occupied by the augend. This instruction is mostly used to modify addresses of instructions and to keep octal counters.
45	TCS	Three character subtract	Similar to the above, but subtraction.
46	LO	Logical OR	Operands are of equal length.
47	LA	Logical AND	Operands are of equal length.
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51	DA	Decimal add	Decimal addition, the operands being of equal, or unequal, length. The result of the addition is stored in the HSM location(s) originally occupied by the augend.
52	DS	Decimal subtract	Similar to the above, but subtraction.
53	DM	Decimal multiply	Decimal multiply. If a quantity is pre-stored in the product area, the product is added (absolute addition) to it, permitting round-off by any number and multiply-accumulate.
54	DD	Decimal divide	Decimal divide. The non-zero-suppressed remainder is stored in the HSM locations originally occupied by the dividend. The operands may be of any length. If the divisor contains more digits than the dividend, the quotient will be zero.
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60			
61	CTC	Conditional transfer of control	This instruction chooses one of three next instructions, according to the setting of the PRI bits. The instruction's A address gives the address of the next instruction to be executed if PRP is set. The B address gives the next instruction if PRN is set. If PRZ is set, the instruction in the location immediately following the CTC order will be executed.
62	SSM	Sense simultaneous mode	This selects one of four next instructions, depending upon whether the Simultaneous Mode is: (a) unoccupied; (b) occupied by a 'read' instruction; (c) occupied by a 'write' instruction; or (d) occupied by a Paper Advance. The next instruction to be executed for case (a) is the one immediately after the SSM order. That for case (b) is held in the A address. That for (c) is in the B address. For case (d), the next instruction to be executed is taken from HSM address 000200.
63	TS	Tape sense	This tests the status of a given Tape Station. The A address gives the address of the next instruction to be executed if the condition being tested is met. The B address gives the Tape Station number and the identity of one of six possible tests of mag tape activity to be performed.
64			
65	SSG	Sense simultaneous gate	This chooses on of two next-instruction addresses, depending upon whether or not the Simultaneous Gate is open. A address is for 'gate open'. B address is for 'gate closed'.
66	TA	Tally	A 'test-and-decrement' instruction. An octal counter is examined. If it is non-zero, the count is decremented and control passed to the address given in the A address. The B address gives the address of the tetrad containing, in its right-most three locations, the counter to be tested.

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71	TC	Transfer control	Unconditional jump, unless the console break-point switches over-ride the jump. The A address gives the location of the next instruction to be executed provided the console switches permit the jump. The B address gives the break-point bits.
72	SET	Set register	Enables a three-character literal to be placed in a selected one of four internal registers. The A address field gives the value of the literal. The B address field specifies one of the following: the PRI registers; the A register; the B register; the T register.
73	STR	Store register	Places the contents of a selected register into the right-most three locations of the specified tetrad. The A address gives the address of the tetrad. The B address field specifies one of the following: the PRI registers; the B register; the P register; the T register.
74			
75	CSG	Control simultaneous gate	This opens or closes the gate which controls entrance into the Simultaneous Mode, making it possible to either prevent or permit simultaneous operations.
76	ST	Stop	Halts the computer, after completion of any instruction in the Simultaneous Mode.
77	RAI	Return after interrupt	This causes a program to be re-entered after an unscheduled interruption, such as for Rollback or for a higher priority program. The contents of the A and B registers are restored.

For the time taken by KDP10 instructions, see *Our Computer Heritage* section N3X2.

KDF8.

Information on the KDF8's instruction set is taken from: *KDF8 Programming Manual.* English Electric publication 1023, 47 pages. It is deduced that the publication date was about 1965.

The KDF8 was marketed as a program-compatible replacement for the KDP10, whilst giving significant [sic] improvements in performance. The KDF8's ferrite core store, known as High Speed memory (HSM), has a cycle time of 12.5 microsecs. whereas the KDP10's cycle time is 15 microsecs. Read or Write transfers between the KDF8 computer and its magnetic tape decks is at the rate of 40K characters/sec., whereas the figures for the KDP10 are: 16K or 33 K characters/sec. when writing; 33K characters/sec. when reading. In all other respects, there is full compatibility between the magnetic tape units (known as Tape Stations) of the KDP10s and KDF8s.

In the KDF8 there has been an enhancement to the Simultaneity, or so-called 'time-sharing', features. Simultaneity for the KDP10 is defined as 'coincident execution of two instructions, both or one of which is an input-output instruction'. This is known as SIMO 1. The KDF8 includes an 'additional simultaneous mode', which allows read/write/compute to be achieved. This is known as SIMO 2. There are consequential changes in the KDF8 to certain registers and the detailed operation of certain instructions. The changes to the registers are noted in *Our Computer Heritage* section N3X2.

Below is the complete instruction set for the KDF8, with the changes to standard KDP10 instructions **noted in blue** and new KDF8 instructions **noted in red**.

Op code	***Mnemonic***	***Instruction***	***Comments***
00			
01	PES	Program error stop	
02	PR	Print	Print one 120-char line
03	PA	Paper advance	Newline on the lineprinter
04	LRR	Linear read reverse	Transfers a message from mag tape or paper tape to HSM.
05	BRR	Block read reverse	Ditto, transferring a block of characters
06	UNS	Unwind n symbols	Moves a selected mag tape forward until a specified number of a designated symbol has been counted
07			
10	TCW	Transcribing card punch write	Same as LW but at half speed (16.7 KC)
11	SSW	Single sector write	Write a sector of any size in block format from HSM to either mag tape or the Monitor Printer.
12	LW	Linear write	Transfers a message from HSM to mag tape, the Monitor Printer or paper tape.
13	MSW	Multiple sector write	Transfers to mag tape (or Monitor Printer) a Block comprising the contents of any Number of sectors taken from the HSM Under the direction of a stored list of Addresses.
14	LRF	Linear read forward	Reads one message from mag tape or Paper tape to HSM.
15	BRF	Block read forward	Reads a block of characters from mag tape Or paper tape to HSM.
16	RNS	Rewind n symbols	Causes a selected mag tape to be moved Backward by a specified number of Symbols.
17	RWD	Rewind to BTC	Causes a selected mag tape to be Completely rewound.
20			
21	IT	Item transfer	Transfers an item from one group of

			Successive HSM locations to another.
22	OCT	One character transfer	Transfers the contents of one HSM Location into another HSM location.
23			
24	STC	Sector transfer by character	Transfers a series of characters from an Area (sector) between, and including, two Designated HSM locations to another HSM Area (sector).
25	TCT	Three character transfer	Transfers, in parallel, the contents of the Right-most three locations of one tetrad to The right-most three locations of another Tetrad in HSM.
26	STT	Sector transfer by tetrad	Transfers the contents of one tetrad or any Number of consecutive HSM tetrads between, and including, two specified tetrad Addresses into another specified tetrad or Consecutive series of tetrads.
27	RD	Random distribute	Distributes successive items in the HSM, to locations specified by a stored list of addresses.
30			
31	LNS	Locate nth symbol in sector	Searches the contents of successive HSM locations between, and including, two give addresses, counting the occurrences of a designated symbol.
32	ZS	Zero suppress	Deleted the non-significant zeros to the left of the MSC of the result of a decimal arithmetic operation.
33	JR	Justify right	Gives right columnar alignment by: (a) adjusting and transferring an item from one series of successive HSM locations to another, or (b) adjusts the item, leaving it in the same group of HSM locations.
34	SCC	Sector clear by character	Places space characters in all the locations between, and including, two HSM addresses.
35	SCR	Sector compress – retain redundant ISS's	Transfers a sector of characters from one part of the HSM to another, in the process removing all spaces located to the right of the right-most non-space character within each item in the sector.
36	SCT	Sector clear by tetrad	Inserts spaces in the HSM locations between, and including, two given tetrad addresses. (Clears four characters at a time).
37	SCD	Sector compress – delete redundant ISS's	Transfers a sector of data from one part of HSM to another. In the process it deletes: (a) all ISSs originally located to the right of the right-most non-ISS, non-space character in the sector, and (b) all spaces located to the right of the right-most non-space character in the sector.
40			
41	BA	Binary add	The operands (assumed numeric) may be of any length but must have the same length.
42	BS	Binary subtract	Ditto
43	SC	Sector compare	Determines the relative magnitude of two operands of equal length. Binary subtraction is performed

			but the difference is not stored in the HSM. However, the resultant PRI settings permit alternative sequences of instructions to be executed.
44	TCA	Three character add	Binary addition of an augend stored in the right-most three locations of a tetrad and a three-character addend. The result is automatically stored in the locations previously occupied by the augend. This instruction is mostly used to modify addresses of instructions and to keep octal counters.
45	TCS	Three character subtract	Similar to the above, but subtraction.
46	LO	Logical OR	Operands are of equal length.
47	LA	Logical AND	Operands are of equal length.
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51	DA	Decimal add	Decimal addition, the operands being of equal, or unequal, length. The result of the addition is stored in the HSM location(s) originally occupied by the augend.
52	DS	Decimal subtract	Similar to the above, but subtraction.
53	DM	Decimal multiply	Decimal multiply. If a quantity is pre-stored in the product area, the product is added (absolute addition) to it, permitting round-off by any number and multiply-accumulate.
54	DD	Decimal divide	Decimal divide. The non-zero-suppressed remainder is stored in the HSM locations originally occupied by the dividend. The operands may be of any length. If the divisor contains more digits than the dividend, the quotient will be zero.
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60	SSO	Sense simultaneous operations	This instruction senses one of three sequences, depending upon whether: (a) Simultaneous Read Mode (SIMO I) and Simultaneous Write Mode (SIMO II) are both occupied; (b) only one of the simultaneous modes is occupied; or (c) both simultaneous modes are unoccupied.
61	CTC	Conditional transfer of control	This instruction chooses one of three next instructions, according to the setting of the PRI bits. The instruction's A address gives the address of the next instruction to be executed if PRP is set. The B address gives the next instruction if PRN is set. If PRZ is set, the instruction in the location immediately following the CTC order will be executed.
62	SSM	Sense simultaneous mode	This selects one of four sequences of instructions, depending upon whether: (a) the Simultaneous Modes are unoccupied; (b) the Simultaneous Read Mode (SIMO I) is occupied by a read instruction; (c) the Simultaneous Write Mode (SIMO II) is occupied by a write instruction; (d) the

			Simultaneous Read Mode (SIMO I) is occupied by a Paper Advance (1033 lineprinter only).
63	TS	Trunk sense	This tests the status of a given Tape Unit or on-line printer (Model 1040) permitting program direction to one of two sequences of instructions.
64	SSG2	Sense simultaneous gate 2.	This instruction chooses one of two sequences of instructions depending upon whether or not the Simultaneous Gate 2 is open.
65	SSG1	Sense simultaneous gate 1	This chooses on of two sequences of instructions, depending upon whether or not the Simultaneous Gate 1 is open.
66	TA	Tally	A 'test-and-decrement' instruction. An octal counter is examined. If it is non-zero, the count is decremented and control passed to the address given in the A address. The B address gives the address of the tetrad containing, in its right-most three locations, the counter to be tested.
67			
70			
71	TC	Transfer control	Unconditional jump, unless the console break-point switches over-ride the jump. The A address gives the location of the next instruction to be executed provided the console switches permit the jump. The B address gives the break-point bits.
72	SET	Set register	Enables a three-character literal to be placed in a selected one of four internal registers. The A address field gives the value of the literal. The B address field specifies one of the following: the PRI registers; the A register; the B register; the T register.
73	STR	Store register	Places the contents of a selected register into the right-most three locations of the specified tetrad. The A address gives the address of the tetrad. The B address field specifies one of seven options, one of which (octal 50) depends upon whether either SIMO I or SIMO II was last activated.
74	CSG (1&2)	Control simultaneous gates 1 and 2	This instruction opens or closes the simultaneous gates to control two- or three- way simultaneity. There are four open/closed options: both open, both closed, gate 2 open & gate 1 closed, gate 2 closed & gate 1 open.
75	CSG 1	Control simultaneous gate 1	This opens or closes the gate which controls two-way simultaneity, making it possible either to prevent or to permit simultaneous operations.
76	ST	Stop	Halts the computer, after completion of any instruction in the Simultaneous Mode.
77	RAI	Return after interrupt	This causes a program to be re-entered after an unscheduled interruption, such as for Rollback or for a higher priority program. The contents of the A and B registers are restored.

For the time taken by KDF8 instructions, see *Our Computer Heritage* section N3X2.